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Effective Timing Error Tolerance Using MSR Logic

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ABSTRACT: Performance changeability in an integrated circuit can basically affect parametric output and product consistency in nanometer technology.As a result, variant tolerance is becoming an essential design requirement, especially for timing decisive applications. Error detection and correction circuit(EDC) reduce delay factors, by the review of the design and resynthesis techniques.The EDC is modified by MUX based self repair(MSR) logic. The simultaneous timing error detection and correction done using multiplexer and inverter with reduction in cost,area and power. MSR logic aims to accomplish high accuracy in the output.

KEYWORDS: Timing errors, Error detection and correction, Timing error tolerance, processVariation, MSR

I. INTRODUCTION

The technology was accomplished as higher levels of integrating the circuit intoundivided Silicon chip directs to Large Scale Integration (LSI), which preceded VLSI. The advantages of VLSI, integration level started to necessitate testing strategies to verify the correct device operation.Testing is a substantiation technique used at the completion stage and examine the deportment of a program by executing the program.Testing should help to locate errors, not just detect their presence.Thedestination of testing is to find and demonstrate faults. The errors occur during the transmission they are (i) Transient Errors (Nonrecurring errors) Caused by external disturbance,e.g. radiation, noise, power disturbance.(ii)Intermittent Errors (Recurring errors) Caused by marginal design parameters 1)Timing problems,e.g. hazards, skew 2)Signal reliability problems, e.g. crosstalk

Error made in writing a program with the underestimating of the time which causes the unnecessary delays in the execution of the program[2].Timing errors are mostlyinduced by the error escape from test, environmental error and operating conditions, are a real disquiet in nanometer technologies[4].Timing errors produce high complexity, multivoltage and multifrequency integrated circuits in nanometer technology. A Timing error detection and correction technique are present in this work that is based on the flip-flop. The error tolerate is done by complementing the turnout of flip flop [3],[6].

The two types of timing errors were occurred during the process they are Type I error is the incorrect rejection of a true e.g.hospital test result shows a patient suffer from a disease instead of patient does not suffer from the disease, a fire alarm going to indicating a fire when there is no fire, or a hospital report suggesting that a medical treatment can cure anillness when it does not.Type II error is the letdown to reject a false, e.g., patient, blood test running out to detect the disease who really has the disease; a fire breaking out that time fire alarm does not ring; or a hospital report indicating that a medical treatment cannot cure a disease when it does.

EDC (Error Detection and Correction) flip flop to find the timing error[13] by comparing the input and turnout of flip flop using comparator, if the output indicates dissimilar from the input difference as error which produce a major problem in receiving the corrected output. The Error was corrected by performing the latch and XOR operation and

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send the turnout of comparator as the error free [12]. MSR (MUX Based Self Repair Logic) logic was proposed with the improvement in the error tolerance with the achievable reduction in area and power[5].

II. EARLIER TIMING ERROR TOLERANCESOLUTIONS

A ERROR DETECTION SYSTEM

The Error is detected by discrepancies in between anestimated and specified, estimated correct value. A flip-flop was a circuithat has two states as stable and employed to store the stable information. A flip-flop is bistable multivibrator and basic establishblocks of digital systems used in computers, communications, and many other types of systems.

Flip-flop was used as a data storage elements. A flip-flop stores data one of its representatives as a "one" and the other represents as a "zero. Flip flop has timed input signals to some reference timing signal.The term flip-flop exclusively for clocked circuits also act as a register, and it said to be as an edge sensitive. Flip flop contents change only on the rise and the fall edge of the enabling signal.The XOR gate wasacting as a comparator that produce a true output (1/HIGH) results when the input and the output were same, otherwise comparator (0/LOW). XOR express the equality and inequality function.

XOR operation can be similar to an addition modulo 2 operation. Other uses of XOR operators are subtractors, comparators, and controlled inverters. XOR gate algebraic operations$(A.\bar{B} + \bar{A}.B)$ were, Inputs A and B.

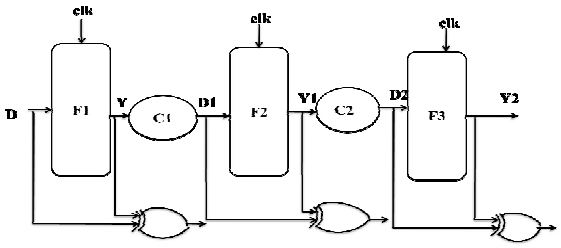

Fig.1.Error Detection Circuit

Fig.1. shows that the timing error was detected by using a comparator to compare the input and output of flip flop, if the output is dissimilar from input means error is occurring in that circuit otherwise the output is free from error.

B ERROR CORRECTION SYSTEM

The Error Correction Flip Flop consists of two XOR gates and one Latch.The first XOR gate acts as a comparator to compare the D input and the output of the Main Flip Flop and passes the output of XOR to the Latch. The Latch receives the first XOR gate an output of the Main Flip-Flop. Latch passes the output of main flip flop to the comparator2. The comparison result of the comparator2 depending on the turnout of the Main Flip Flop and propagated to the output. If the first comparator produce o/low value the latch just passing the output of comparator 1 to the comparator2 based on the reset and clock.. The comparator2 output is considered as the correct and the final output of the EDC Flip Flop. The comparator 1 acts as a control signal, the latch transmits input to output when reset is 1, a clock signal is positive.

Initially, the output of the Latch is reset to zero so that by default the Y signal of the Main Flip-Flop propagates to the output correct of the XOR gate and feeds the subsequent logic stage. In the error free instance the comparator produces the comparison result as a low value on the Comparator output of the first XOR gate after the triggering edge of the clock signal CLK. This value is captured by the Latch. Thus, the correct output signal is identical to the Y signal of the Main Flip- Flop, which carries the correct value. This signal feeds the subsequent logic stage Sj+1.

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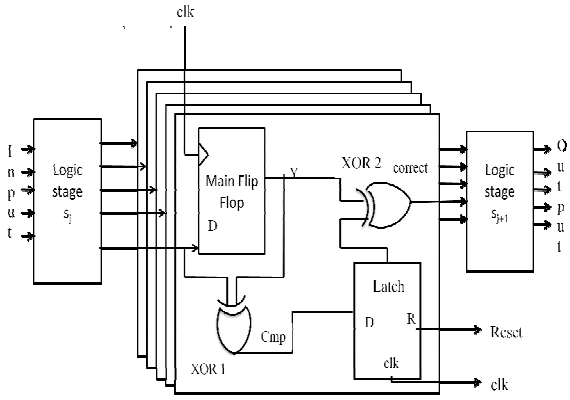

Fig.2.Error Detection and Correction Circuit

Fig.2. shows that the presence of a timing error in main flip flop output, a delayed signal was arriving at the output after the triggering edge of the clock signal CLK. In that case, a timing error is present at the F output of the Main Flip-Flop and erroneous data are provided to the subsequent logic stage Sj+1 through the CORRECT output. In addition, the F signal value differs from the D signal value. The first XOR gate detects this difference and raises its output Comparator to high. The Latch captures and holds this response. Thus, the second XOR gate provides at its output CORRECT the complement of the F signal. Now the CORRECT output of the EDC Flip-Flop carries the correct value, which feeds the subsequent logic stage Sj+1 for its computationConsequently, the error is locally corrected.

A timing error tolerance technique is presented in this work for enhanced reliability in flip-flop based nanometer technology cores. It exploits a new bit flip-flop, which provides the ability to detect and correct multiple timing errors in a circuit, with a time penalty of a single clock cycle.

The input of the error correction should be same as the output correct. Timing delay isa critical one because it considers the wrong value so timing error tolerance is required.

III PROPOSED SOLUTION

A ERROR DETECTION CIRCUIT

The proposed flip-flop detects late-arriving data by comparing the flip-flop using XOR gate as a comparator. The flip-flop get enable/disable based on the clock pulse, it actsas anedge sensitive to signal changes and work as basic clock pulse.

The XOR gate isacting as a comparator that produce a true output (1/HIGH) results when the input and the output were same, otherwise comparator (0/LOW).

XOR express the equality and inequality function.XOR operation can be similar to an addition modulo 2 operation. Other uses of XOR operators are subtractions, comparators, and controlled inverters. XOR gate algebraic operations$(A.\bar{B} + \bar{A}.B)$where A and B are Inputs.

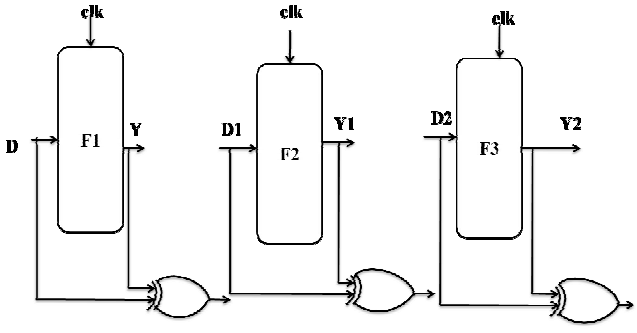

Fig.3. Error Detection Circuit

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Fig.3. shows that the timing error was detected by using a comparator to compare the input and output of flip flop, if the output is dissimilar from input means error is occurring in that circuit otherwise the output is free from error as shown in Fig.3.

B. ERROR CORRECTION CIRCUIT OF MUX BASED SELF REPAIR LOGIC

In this project we present a new timing error detection and correction circuit that delivers fast response times with the use of a MUX and inverter.

The flip flop is edge sensitive and only changes state when a control signal goes from high to low or low to high. Flip flop content is changed only at the rise and fall edge of the enable signal.

A multiplexer (MUX) is to select n number of analog or digital input signals and send selected input into a single line. A multiplexer 2^n inputs have *n* select lines and send selected inputs into the output. Multiplexers are mainly used to increase the amount of data that can be imported over the network within a certain amount of time and the bandwidth. A multiplexer is also called a data selector and used to implement the Boolean functions of multiple variables and gates.

MUX is based on selection line. The XOR output is considered as the selected line of MUX and the MUX getting enable or disable. An inverter or NOT gate is a logic gate which implements logical negation. If the XOR output is high means the MUX get enable and send the inversion of flip flop output to the final output as CORRECT

If the XOR output is considered as the low means the MUX sends the main flip flop output to the final as CORRECT.

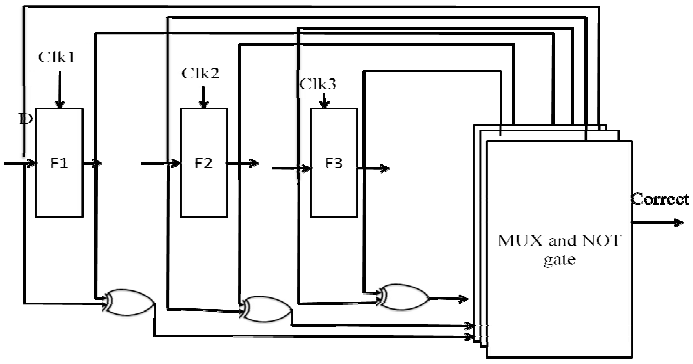

Fig.4. Error Correction Circuit

Fig.4. shows that the main character and an advantage of the proposed topology is that no circuitry is inserted in the critical path from the *D* input to the *CORRECT* output of the Flip-Flop or in the distribution path of the clock signal *CLK*.

IV. SIMULATION RESULT AND ANALYSIS

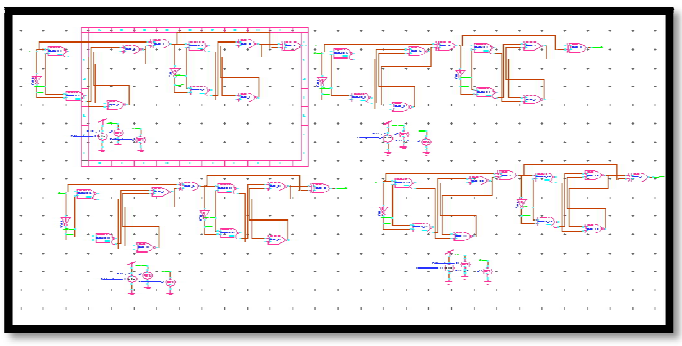

Fig.5. schematic diagram of 4 Bit Error Detection and correction Circuit

Fig.5. shows that the AND gate, XOR gate, flip- flop,latch is used. We have used the faster gate implementation

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using the library files. This requires a numberof inputs and n numberof outputs. The error was detected by the comparator, comparator output was acting as a selection line for enabling/ disabling the latch.XOR express the equality and inequality function. XOR operation can be similar to an addition modulo 2 operation. Other uses of XOR operators are subtractions, comparators, and controlled inverters. XOR gate algebraic operations $(A.\bar{B} + \bar{A}.B)$where A and B are Inputs.A Second comparator compares and produce the final output as a corrective. Control line is used to control the error occurrence during the transmission.

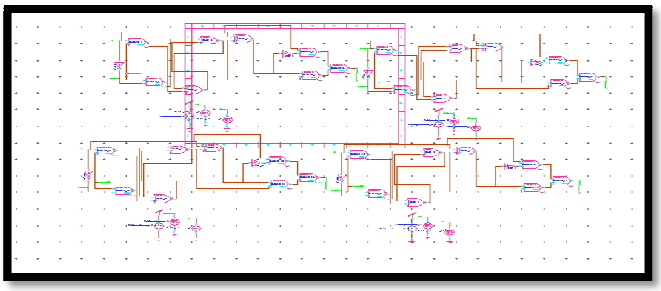

Fig.6. schematic diagram of 4 Bit Of Error Detection and correction Circuit.

Fig.6. Shows the error detection and correction of multiplexer based self repair logic.This requires n numberof inputs and n numberof outputs. The error was detected by the comparator, comparator output was acting as a selection line for enabling/ disabling the MUX. A multiplexer 2^n inputs have *n* select lines and send selected inputs into the output.If an error is occurring means MUX get enable and transmit the input to output after the inversion.

In this segment simulation result for Timing error tolerance using Xilinx 13.2. The d, reset,f are the input and y is the output. Input d was same as the Y when reset is 0. They some delay were occurred during the transmission that was said to be as error. The delay was considered as the wrong pattern.

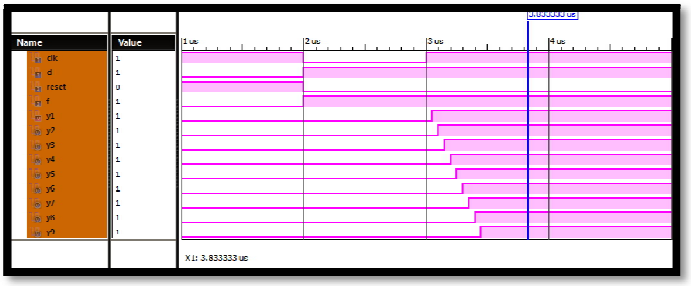

Fig.7.Simulation result of EDC With Fault

Fig.7. shows that the delay occurrence during the transmission from the source or input to the destination or output. The delay is indicated by XOR.

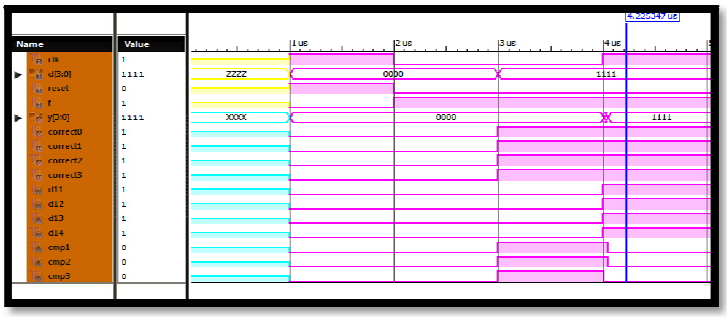

Fig.8. Simulation result of 4BIT Error Detectionand Correction Circuit

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Fig.8. shows that the d,reset are the input and y is the output. Input d was same as the Y when reset is 0.They some delay were occurred during the transmission that was said to be as error. The control output is used to detect the errors, correct output is used to correct the error and produce the output by using the modified technique MSR (Multiplexer Based Self Repair) logic. For Fig.9. Represent 4 Bit EDC

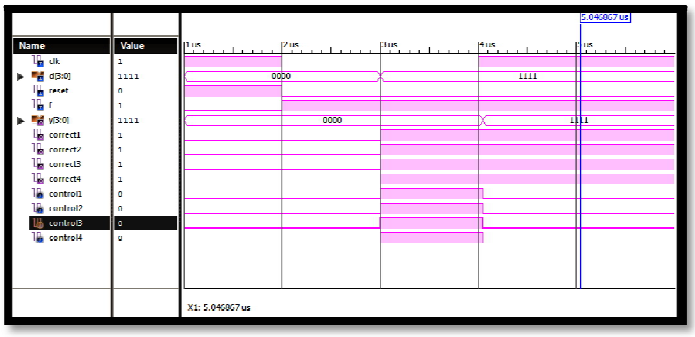

Fig.9. Simulation result of 4 BIT MSR Logic Based EDC Simulation

Fig.9.shows that the area occurs or requirements are analyzed in the Xilinx 13.2 by the slices, LUT, flip-flop,input and output bond. The Gclock clock signal is used to enable otherwise disable the flip-flop operation.

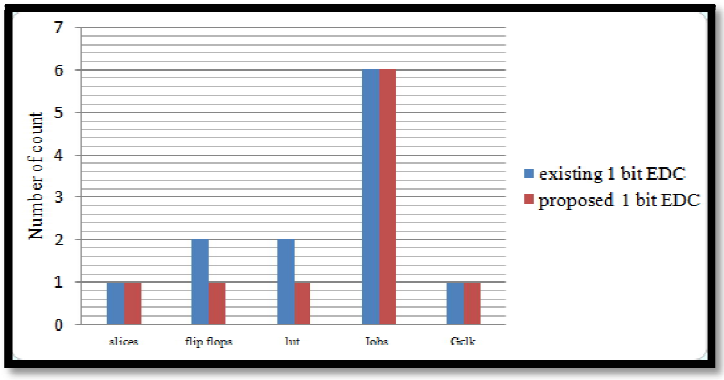

Fig.10.(a)Area Analysis of 1BIT Error Detection and Correction circuit

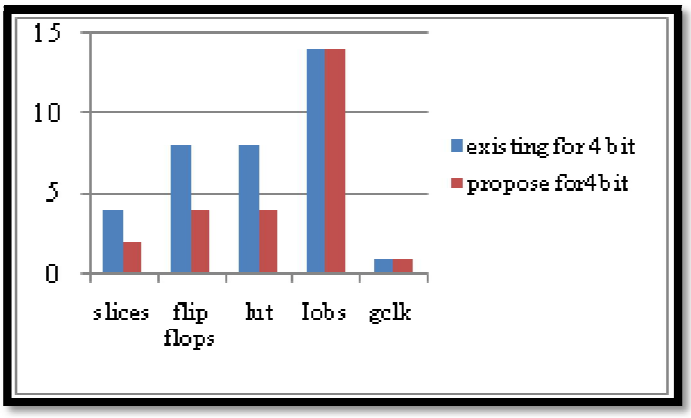

Fig.10.(b) Area Analysis of 4BITof Error Detection and Correction circuit

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Fig. 10(a) shows the 1 bit power analysis for existing and proposed. Fig.10(b). Represent the 4 bit power analysis for EDC and MSR logic.

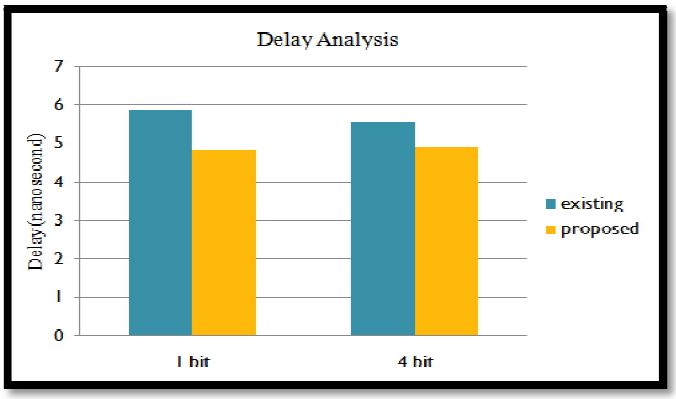

Fig.12.Delay Analysis of 1 bit and 4 bit of existing and proposed.

Fig.12. shows that the delay analysis of the existing and proposed of1 bit and 4 bit.

V. APPLICATION OF EDC

Error Detection and Correction circuit were implemented in the router circuit. A router is a device that forwards data packets in between two different networks. Routing is performed for public switched telephone network, electronic data networks and transportation networks. A data packet is typically forwarded from one router to another through the networks that constitute the internetwork until it reaches its destination node. When a node on one network needs to send a message to a node on another network, this packet will be picked up by the router and passed on to the other network. Many nodes are programmed with a so-called 'default gateway', which is the address of the router that is to take care of all packets not for other nodes on the same network. Home and small office networking are becoming popular by day by the use of IP wired and wireless router.

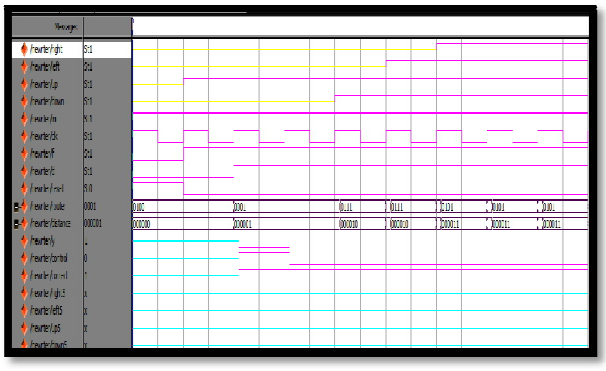

Fig.13.simulation Result of EDC Router Application

Fig.13.shows that the routing was simulated, control the errors during the transmission in between the source to the destination. After the error correction the output was transmitted into the output as the CORRECT output. Wired and wireless router are able to maintain routing and configuration information in their routing table. They also provide the service of filtering traffic of incoming and outgoing packets based on IP address.

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VI. CONCLUSION

In this project, a detecting and correcting concurrent soft and timing errors are presented. It uses minimum hardware overhead logic circuits to detect the erroneous responses at the outputs of the functional circuit being monitored. The earlier error detection and correction method provides error correction as non accurate. The adopted MSR approach can deliver very fast detection times compared to the techniques presented earlier in the literature. It exploits a new MSR logic which provides the ability to detect and correct multiple timing errors during the communication or transmission of information. The EDC circuit will be implemented in the router application. The MSR logic import accurate output with reduction in component and time consuming.

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